"Reprogrammable Instruction DSP"

Robert Osann, Jr., 10494 Ann Arbor Ave., Cupertino, CA 95014, 408-313-1990, Bob@Osann.com

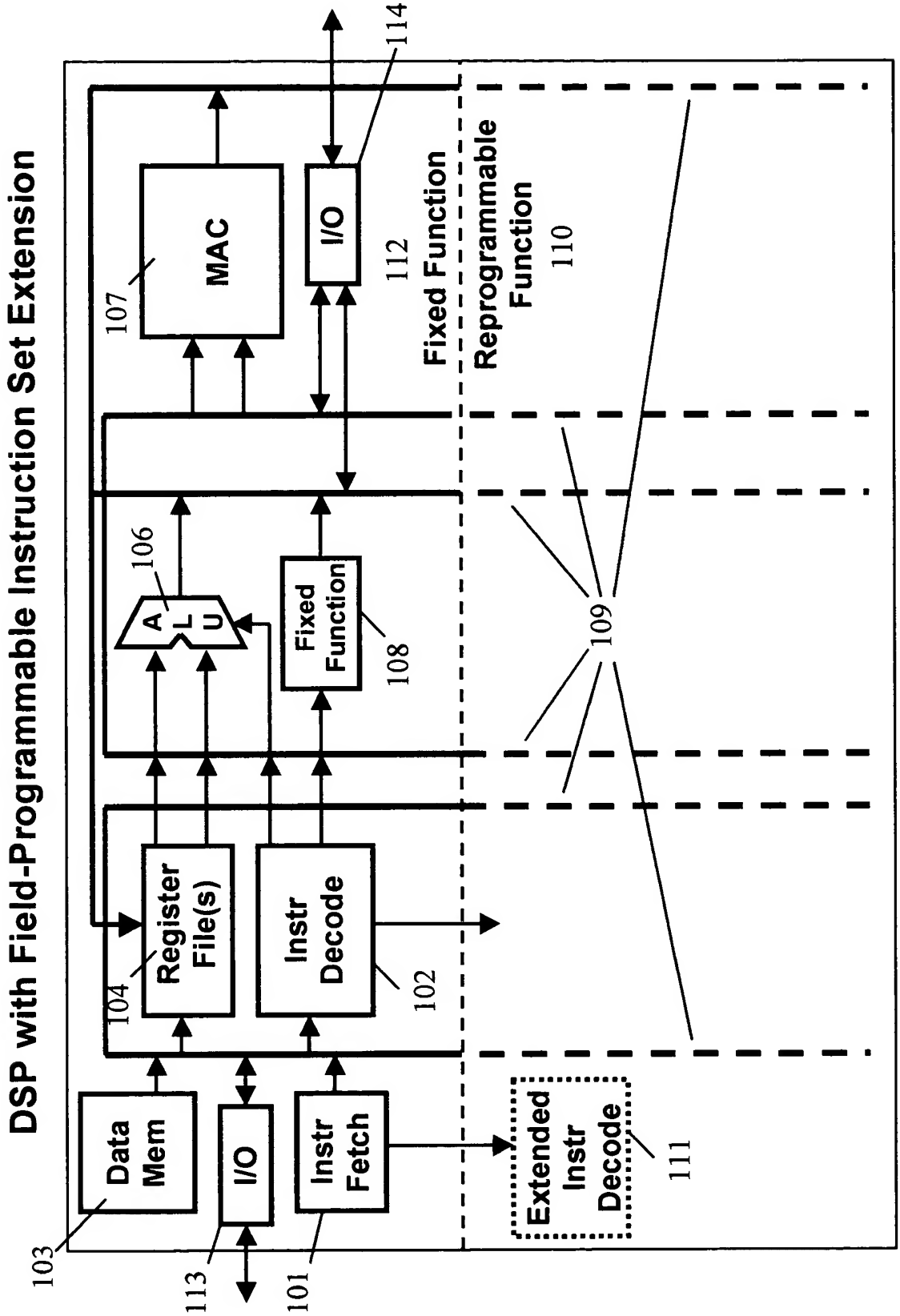


Figure 1

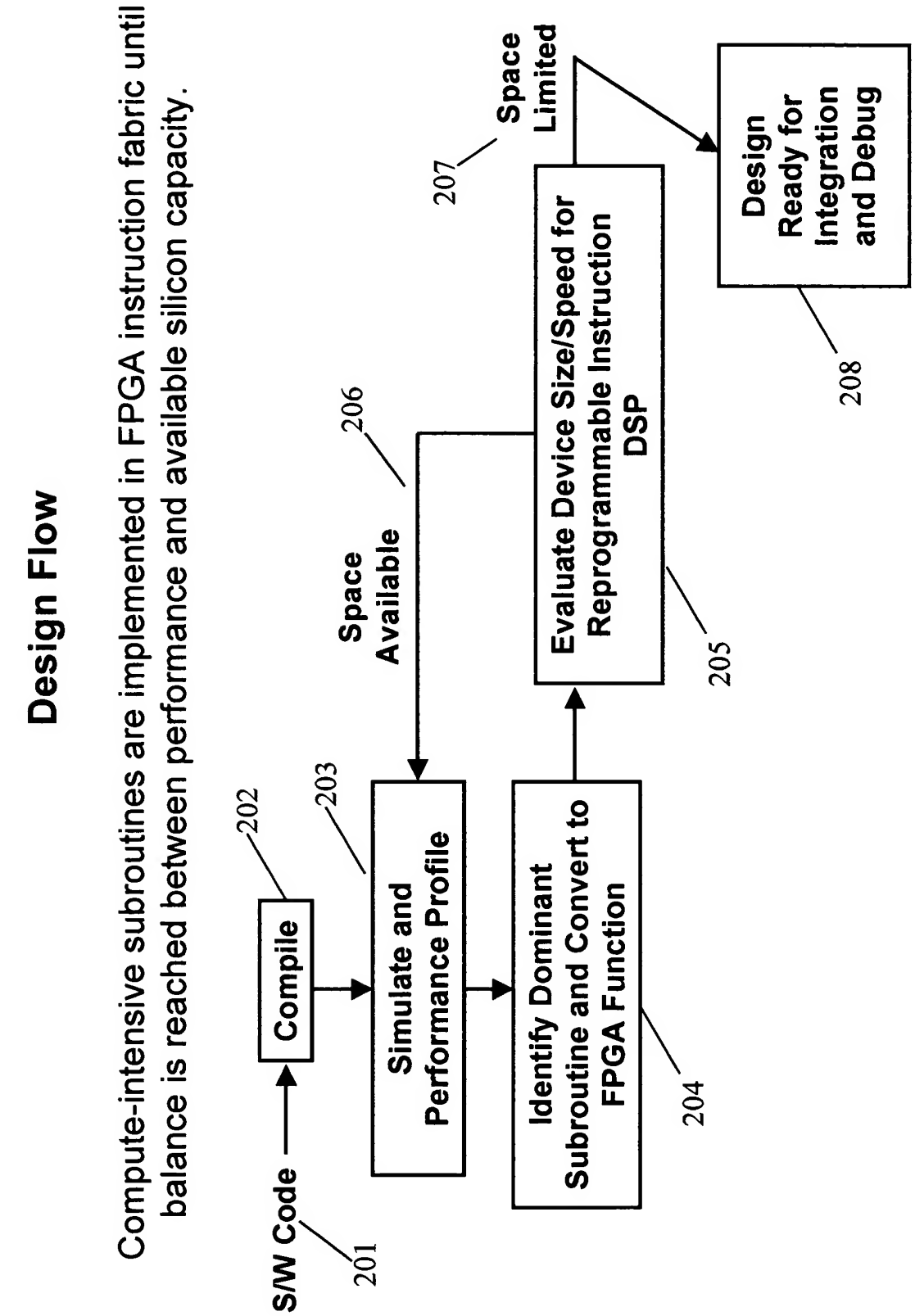
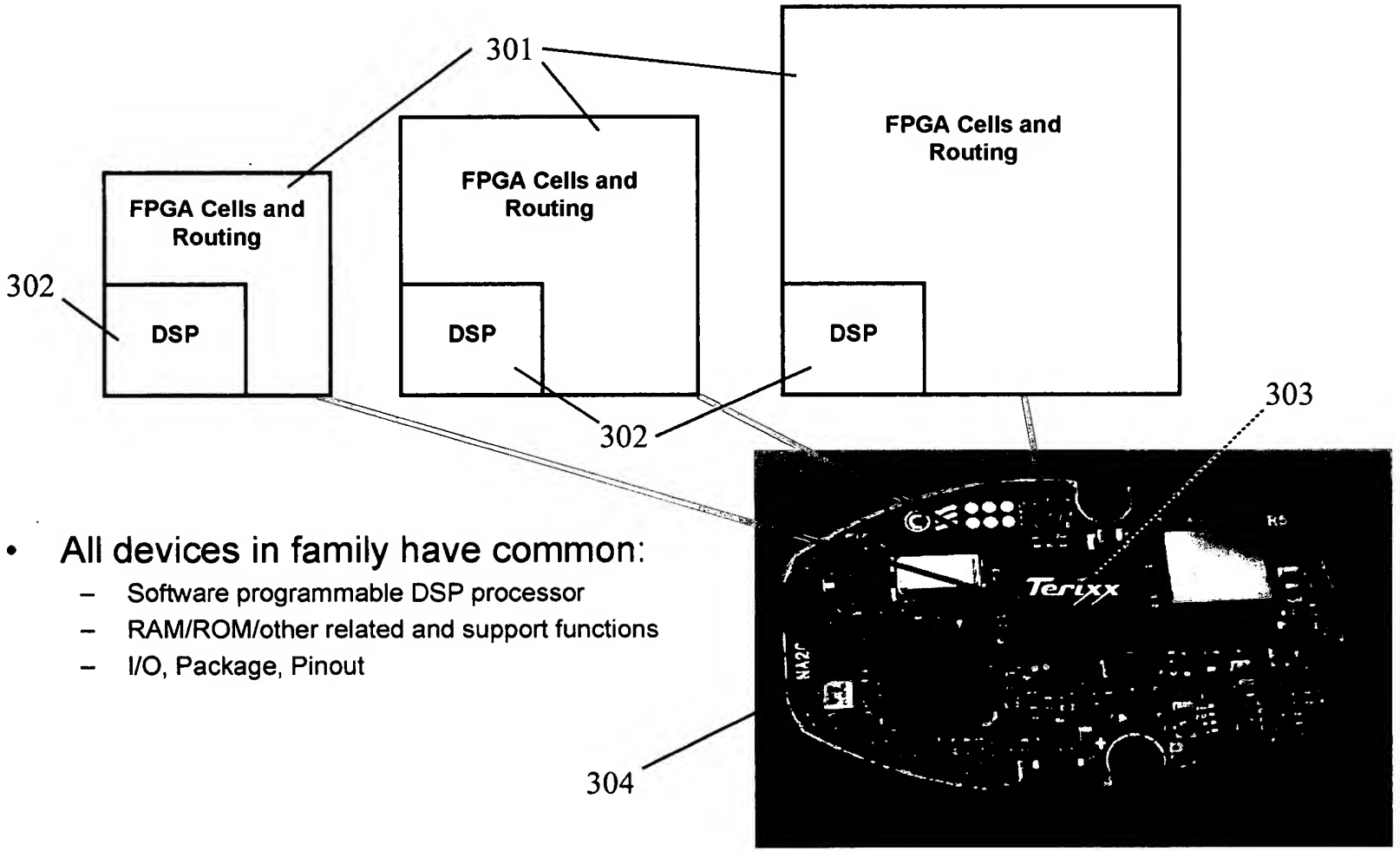

Design Flow
Compute-intensive subroutines are implemented in FPGA instruction fabric until balance is reached between performance and available silicon capacity.
S/W Code
201
Compile
202
Simulate and Performance Profile
203
Identify Dominant Subroutine and Convert to FPGA Function
204
Evaluate Device Size/Speed for Reprogrammable Instruction DSP
205
Space Available
206
Space Limited
207
Design Ready for Integration and Debug
208

Figure 2

Family of Reprogrammable Instruction DSPs



- All devices in family have common:
  - Software programmable DSP processor
  - RAM/ROM/other related and support functions
  - I/O, Package, Pinout

Figure 3

"Reprogrammable Instruction DSP"
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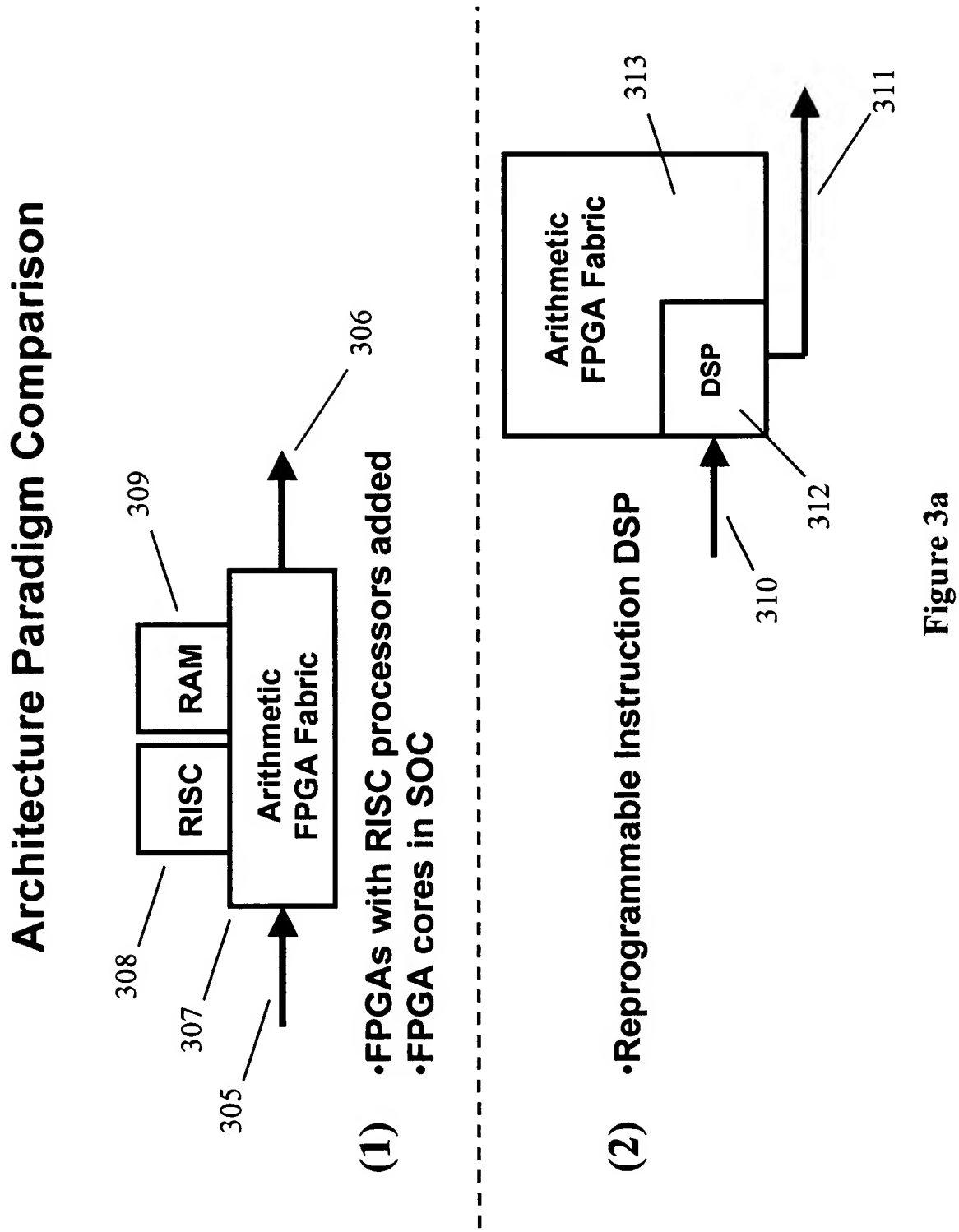
Architecture Paradigm Comparison
(1) •FPGAs with RISC processors added
•FPGA cores in SOC
RISC
RAM
Arithmetic FPGA Fabric
305
307
308
309
306
(2) •Reprogrammable Instruction DSP
Arithmetic FPGA Fabric
DSP
310
312
313
311

Figure 3a

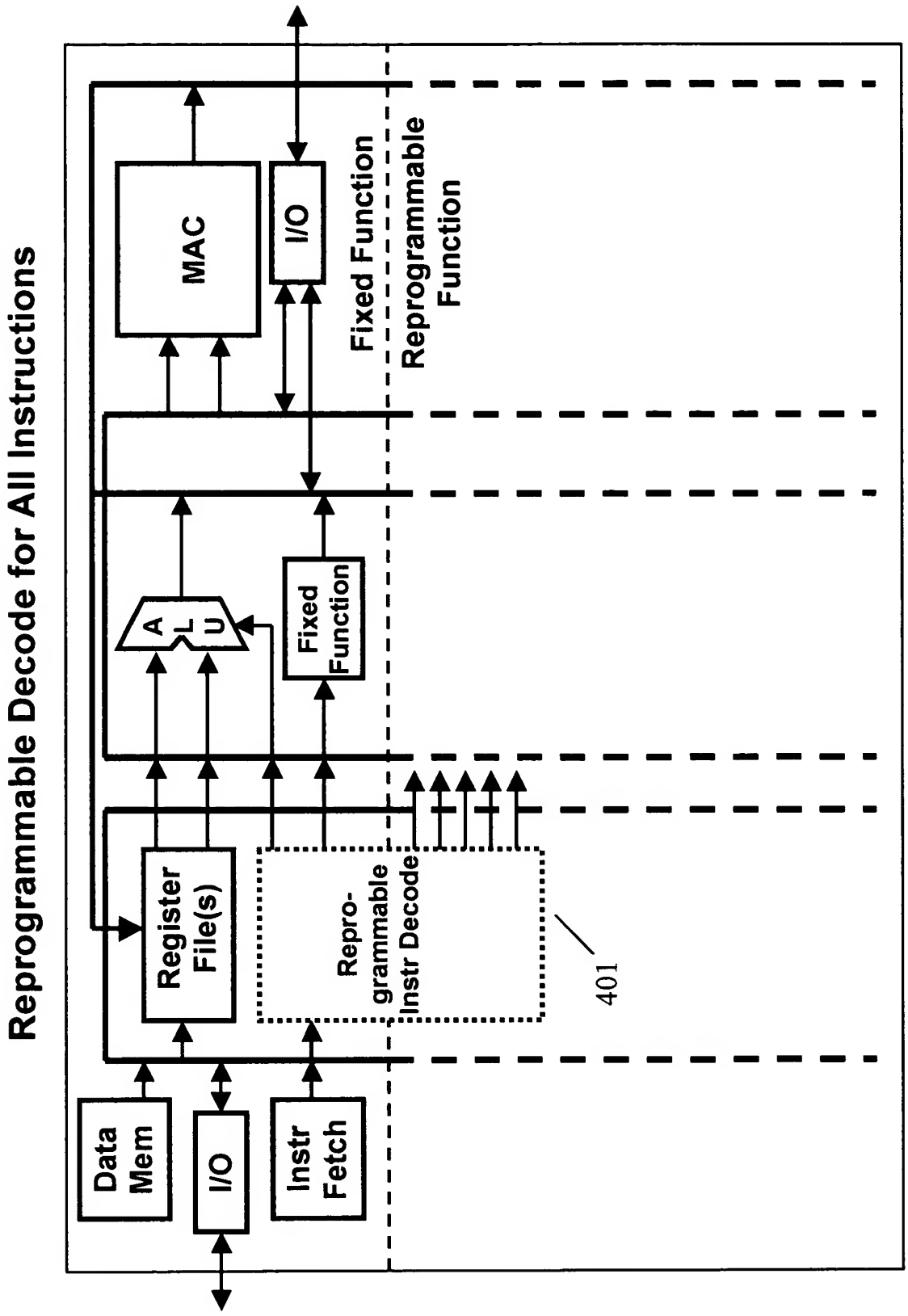
Reprogrammable Decode for All Instructions
MAC
I/O
Fixed Function
Reprogrammable Function
A L U
Fixed Function
Register File(s)
Repro-grammable Instr Decode
401
Data Mem
I/O
Instr Fetch

Figure 4

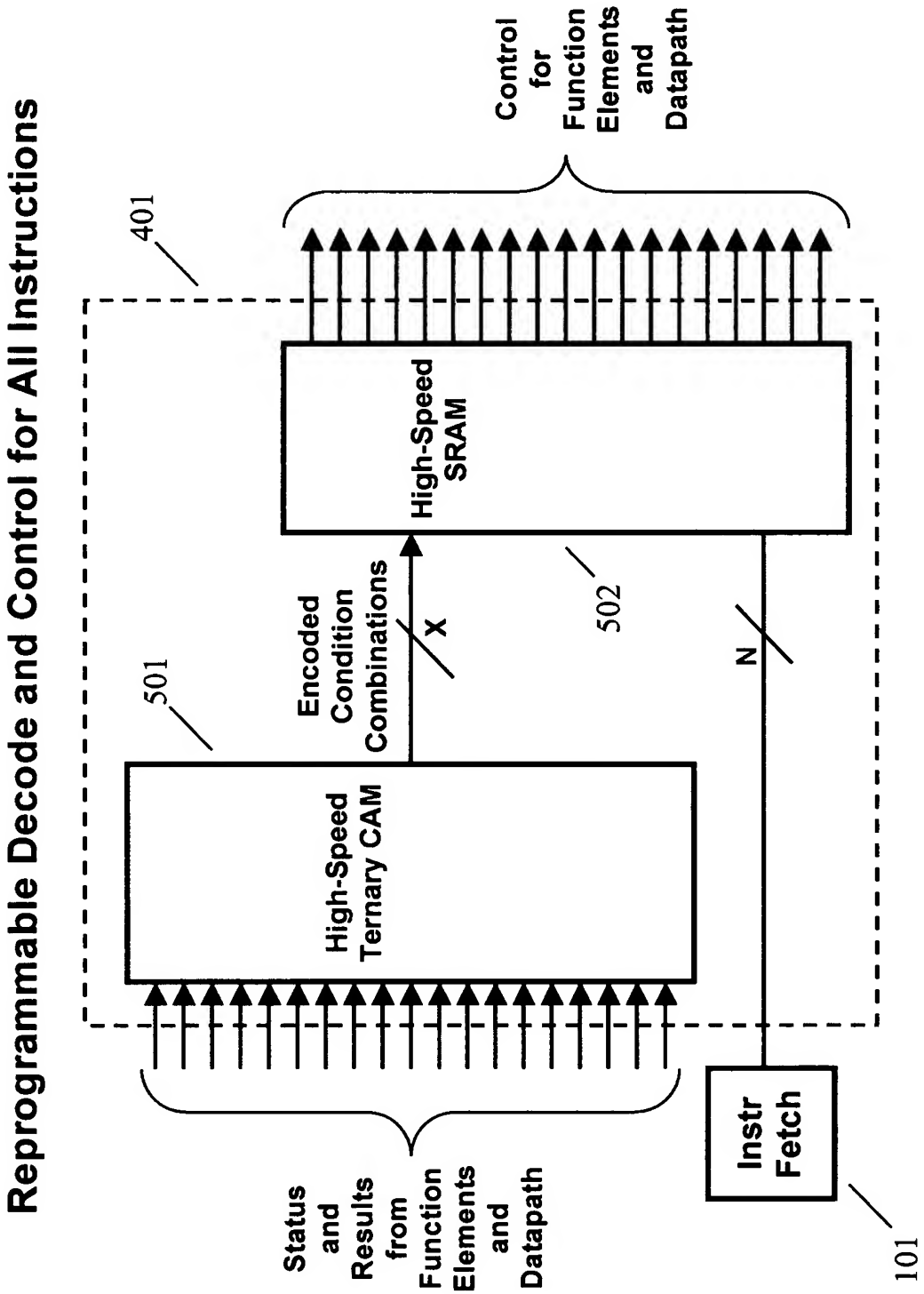
Reprogrammable Decode and Control for All Instructions
401
Control for Function Elements and Datapath
High-Speed SRAM
502
Encoded Condition Combinations
X
N
501
High-Speed Ternary CAM
Status and Results from Function Elements and Datapath
Instr Fetch
101

Figure 5

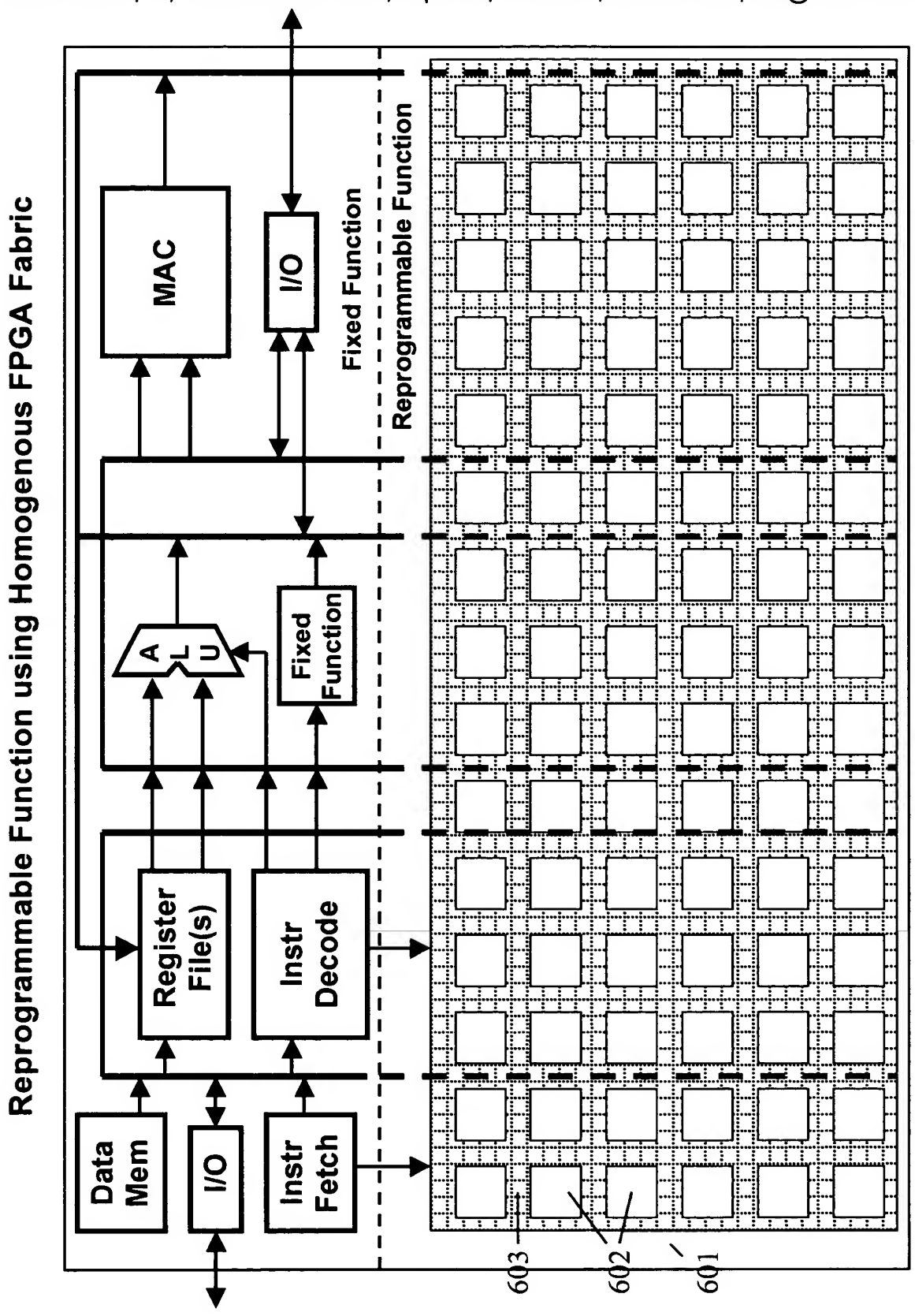
Reprogrammable Function using Homogenous FPGA Fabric
Fixed Function
Reprogrammable Function
MAC
I/O
A
L
U
Fixed Function
Register File(s)
Instr Decode
Data Mem
I/O
Instr Fetch
603
602
601

Figure 6

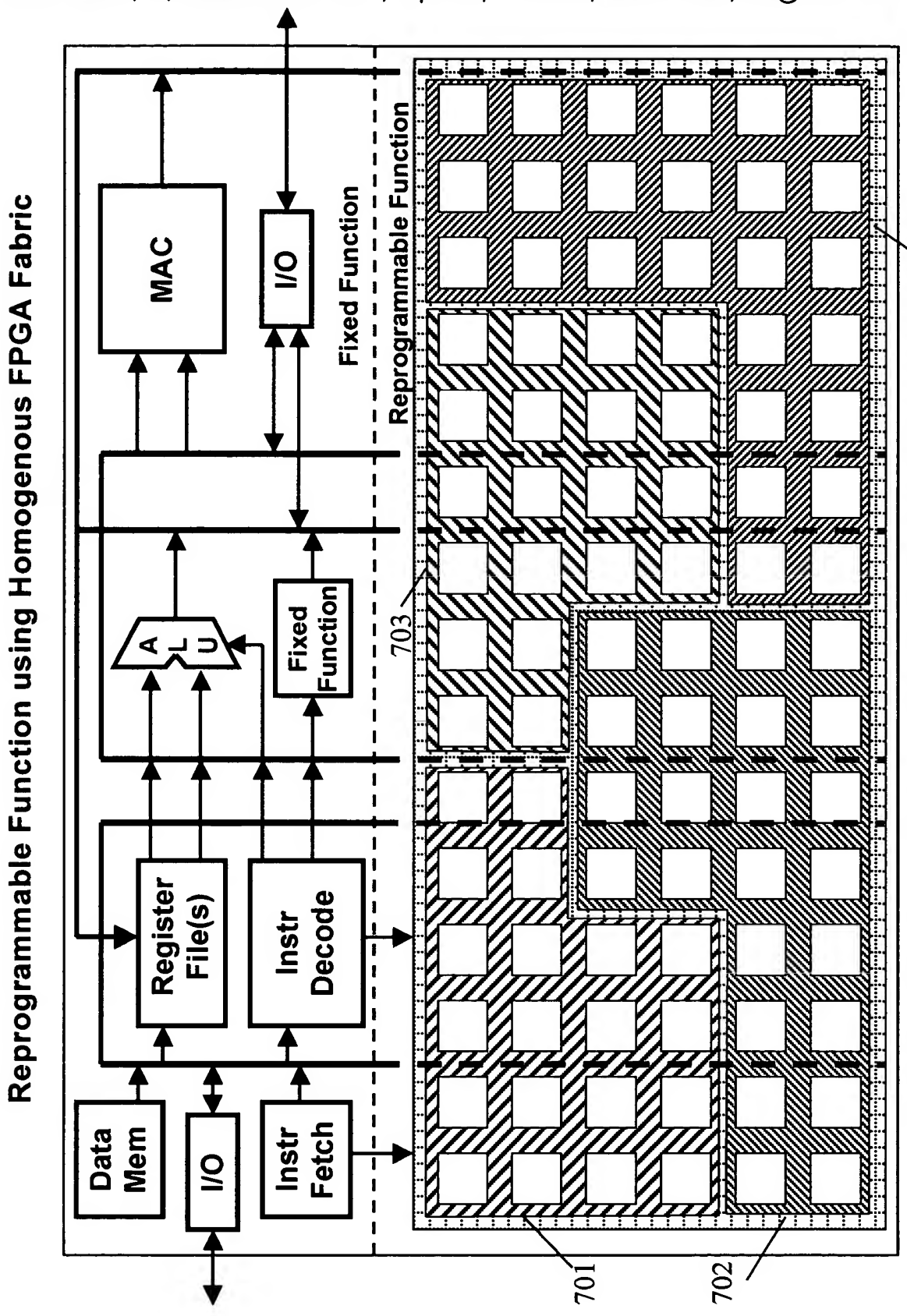
Reprogrammable Function using Homogenous FPGA Fabric
Fixed Function
Reprogrammable Function
MAC
I/O
A
L
U
Fixed Function
Register File(s)
Instr Decode
Data Mem
I/O
Instr Fetch
703
704
701
702

Figure 7

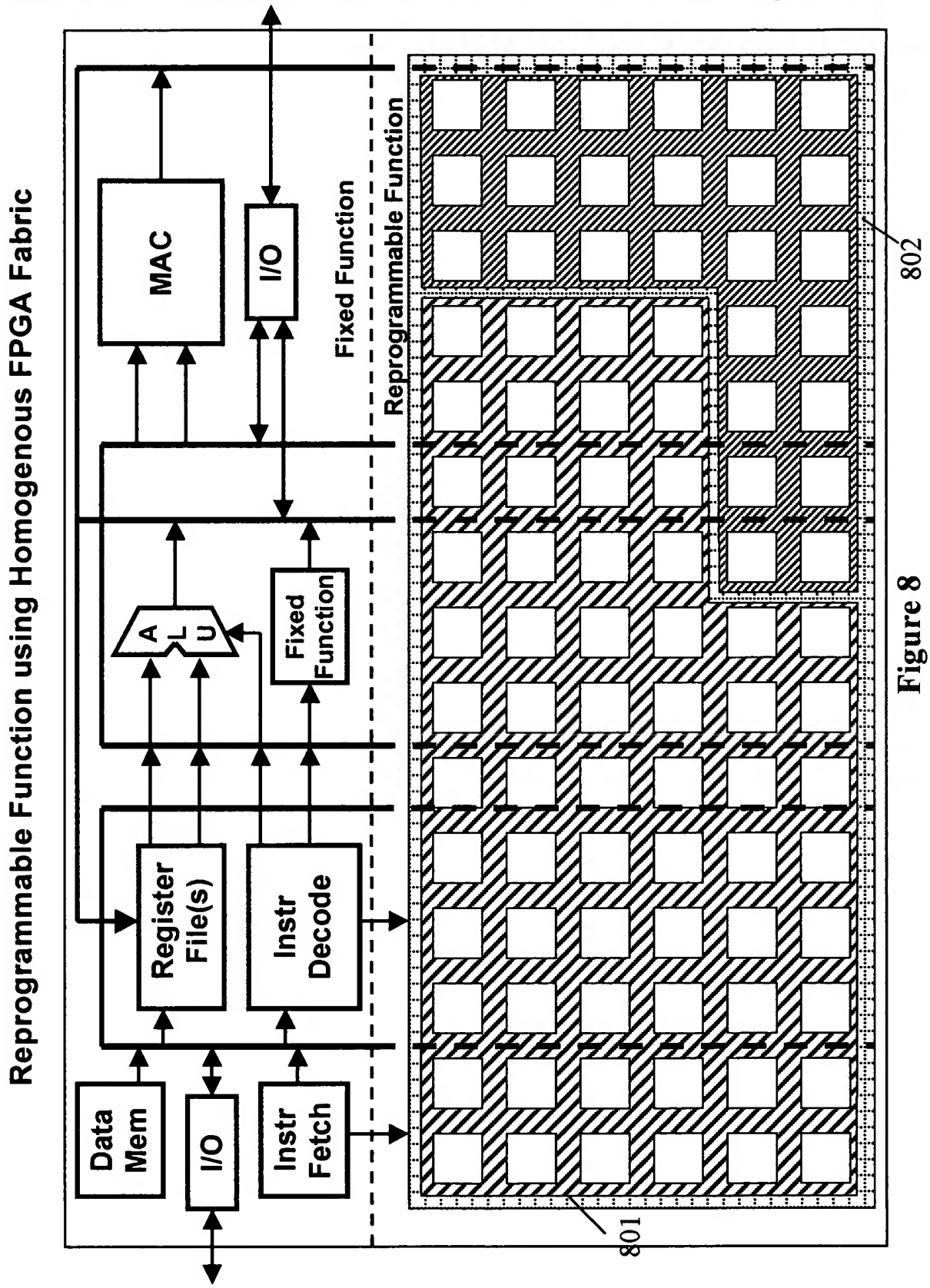
Reprogrammable Function using Homogenous FPGA Fabric
MAC
I/O
Fixed Function
Reprogrammable Function
A
L
U
Fixed Function
Register File(s)
Instr Decode
Data Mem
I/O
Instr Fetch
801
802

Figure 8

"Reprogrammable Instruction DSP"

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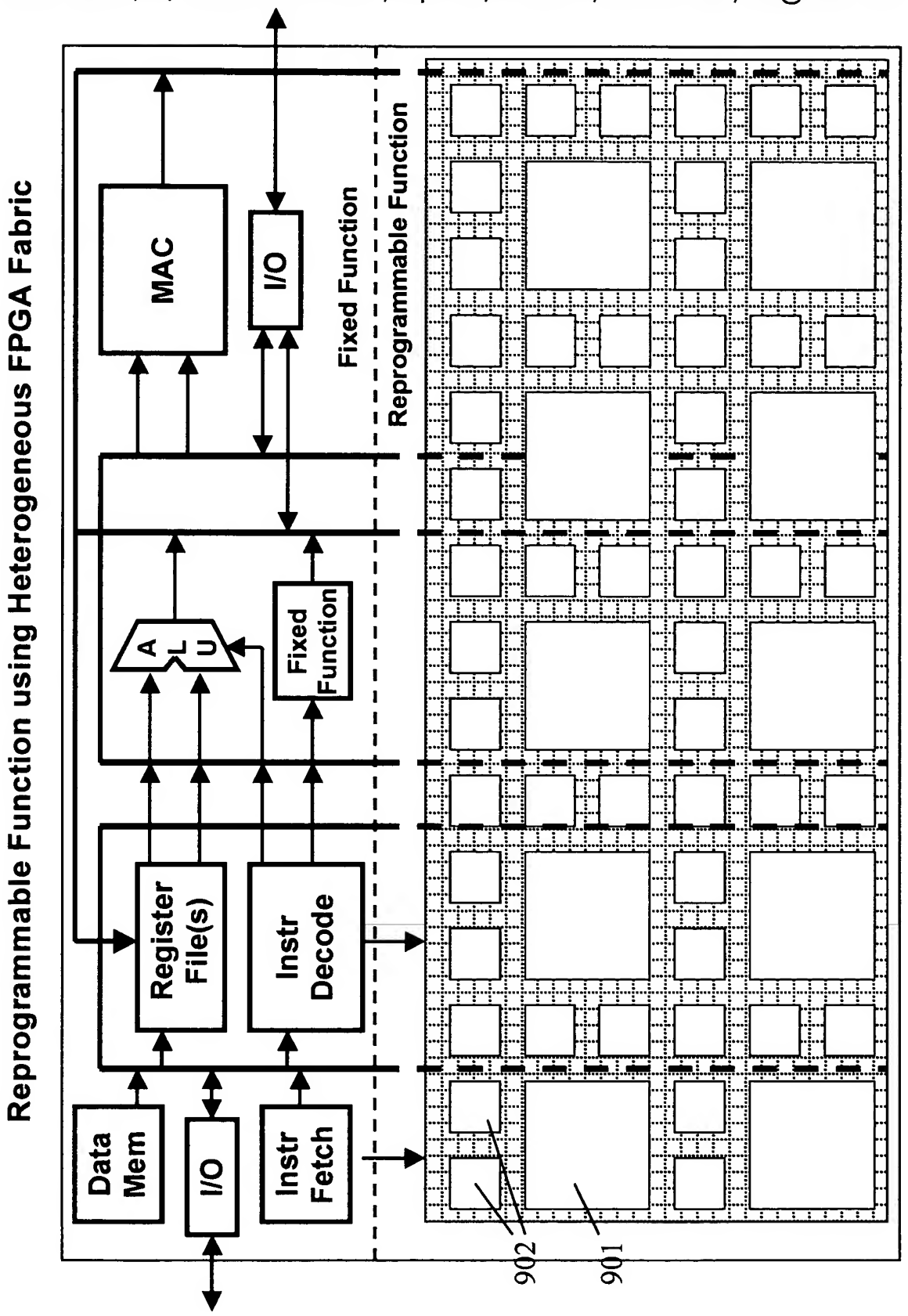

Figure 9

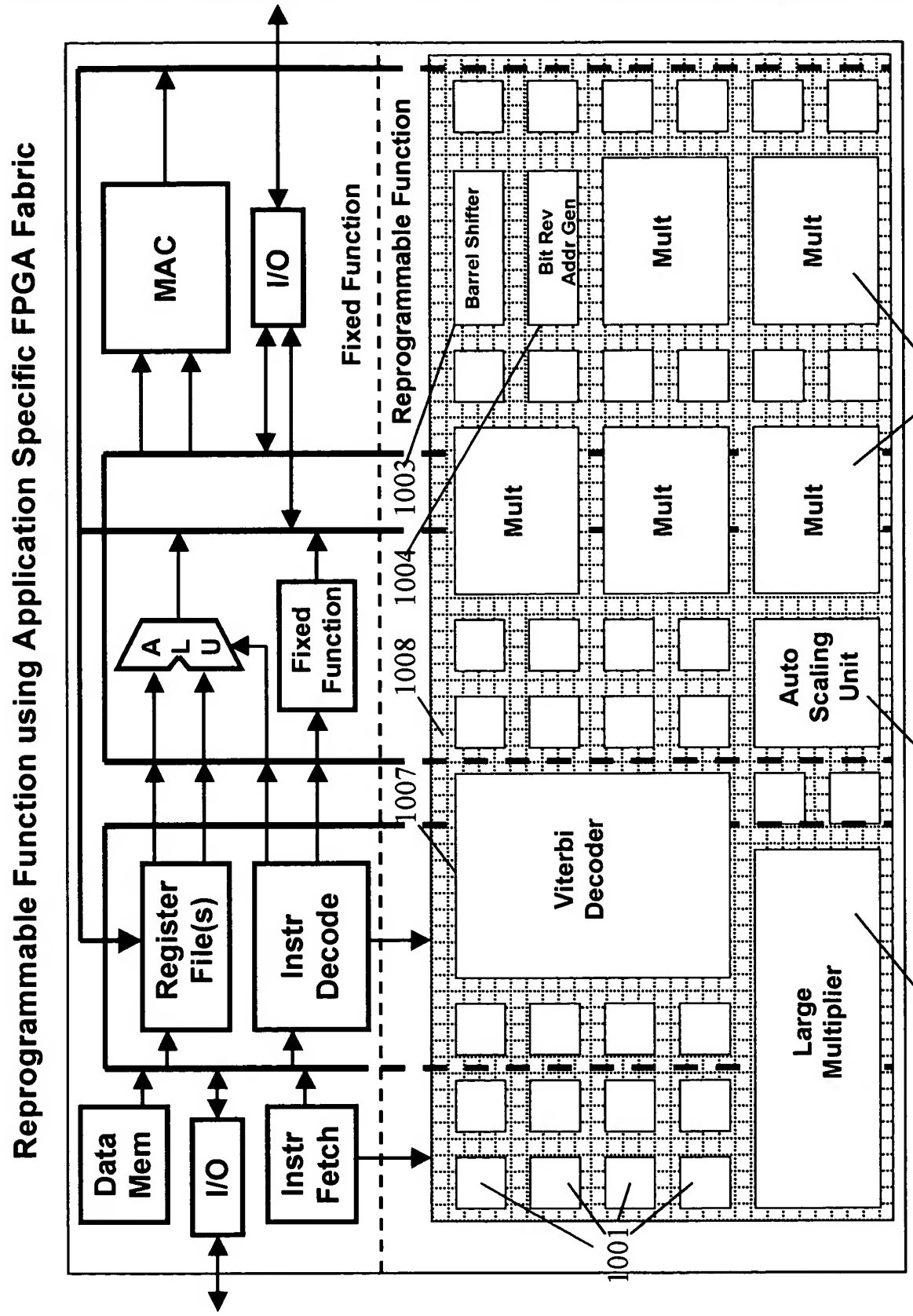
Reprogrammable Function using Application Specific FPGA Fabric
Fixed Function
Reprogrammable Function
MAC
I/O
A
L
U
Fixed Function
Register File(s)
Instr Decode
Data Mem
I/O
Instr Fetch
Barrel Shifter
Bit Rev Addr Gen
Mult
Mult
Mult
Mult
Mult
Auto Scaling Unit
Viterbi Decoder
Large Multiplier
1001
1002
1003
1004
1005
1006
1007
1008

Figure 10

Types of FPGA Fabric

Heterogeneous FPGA Fabric:

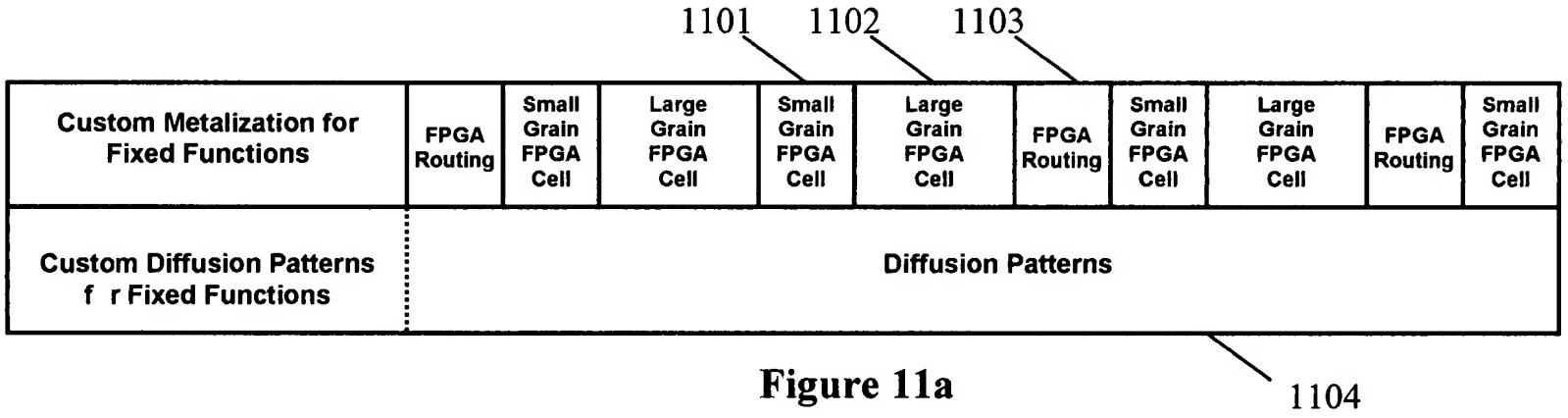

Figure 11a

Application-Specific FPGA Fabric:

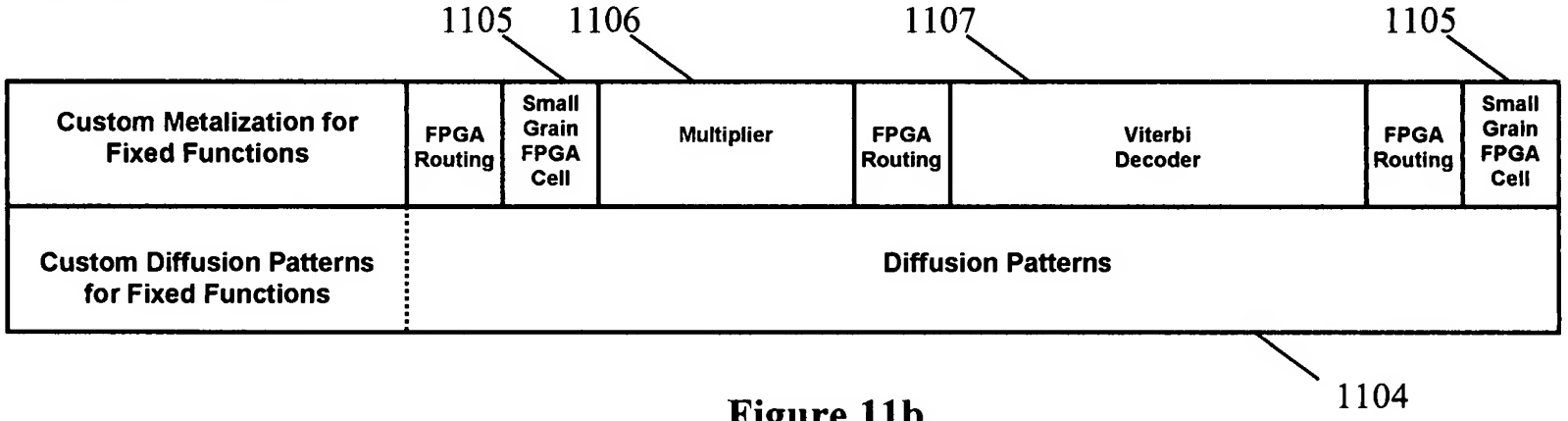

Figure 11b

"Reprogrammable Instruction DSP"
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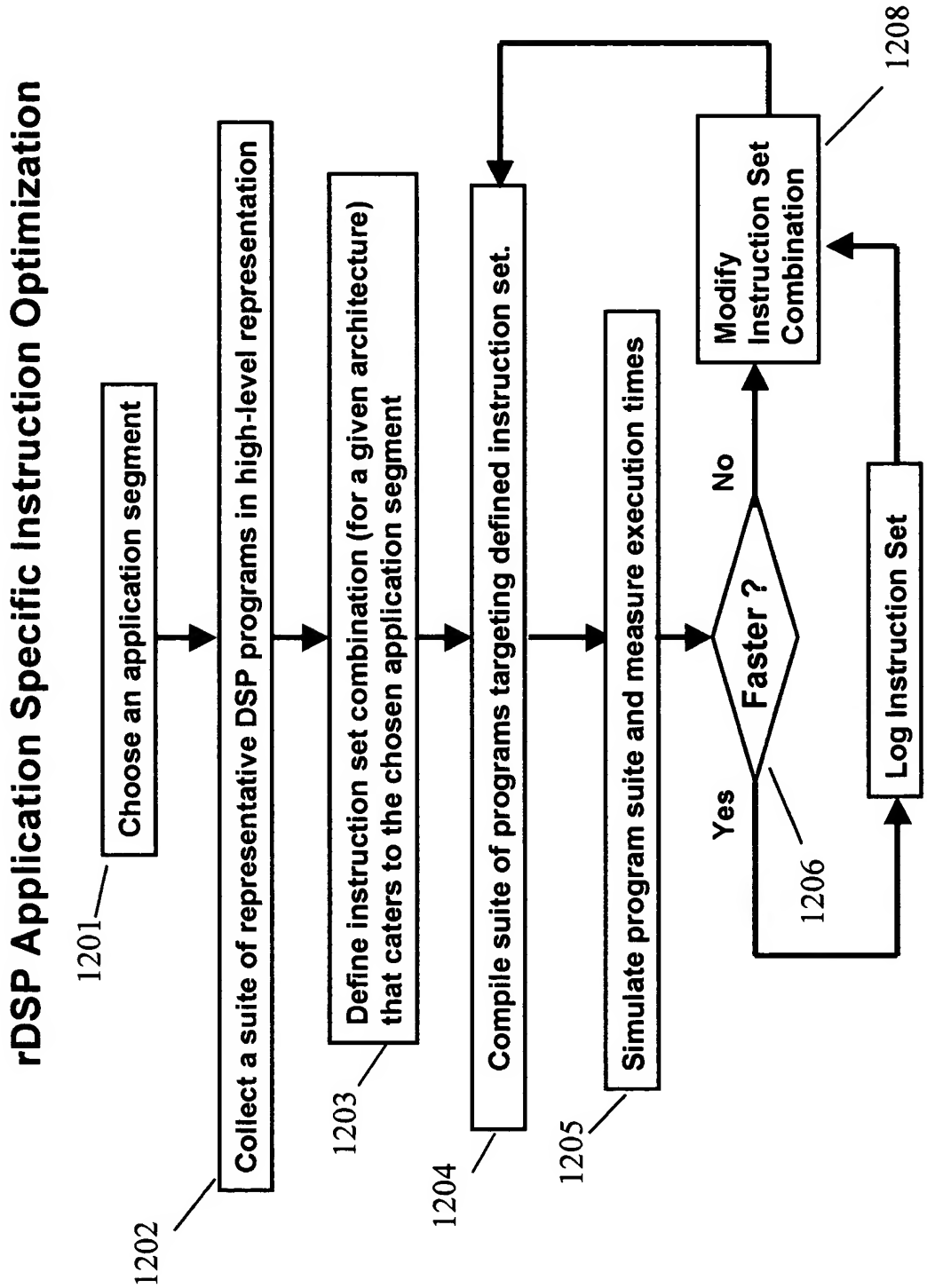
rDSP Application Specific Instruction Optimization
Choose an application segment
1201
Collect a suite of representative DSP programs in high-level representation
1202
Define instruction set combination (for a given architecture) that caters to the chosen application segment
1203
Compile suite of programs targeting defined instruction set.
1204
Simulate program suite and measure execution times
1205
Faster ?
Yes
No
1206
Log Instruction Set
1207
Modify Instruction Set Combination
1208

Figure 12

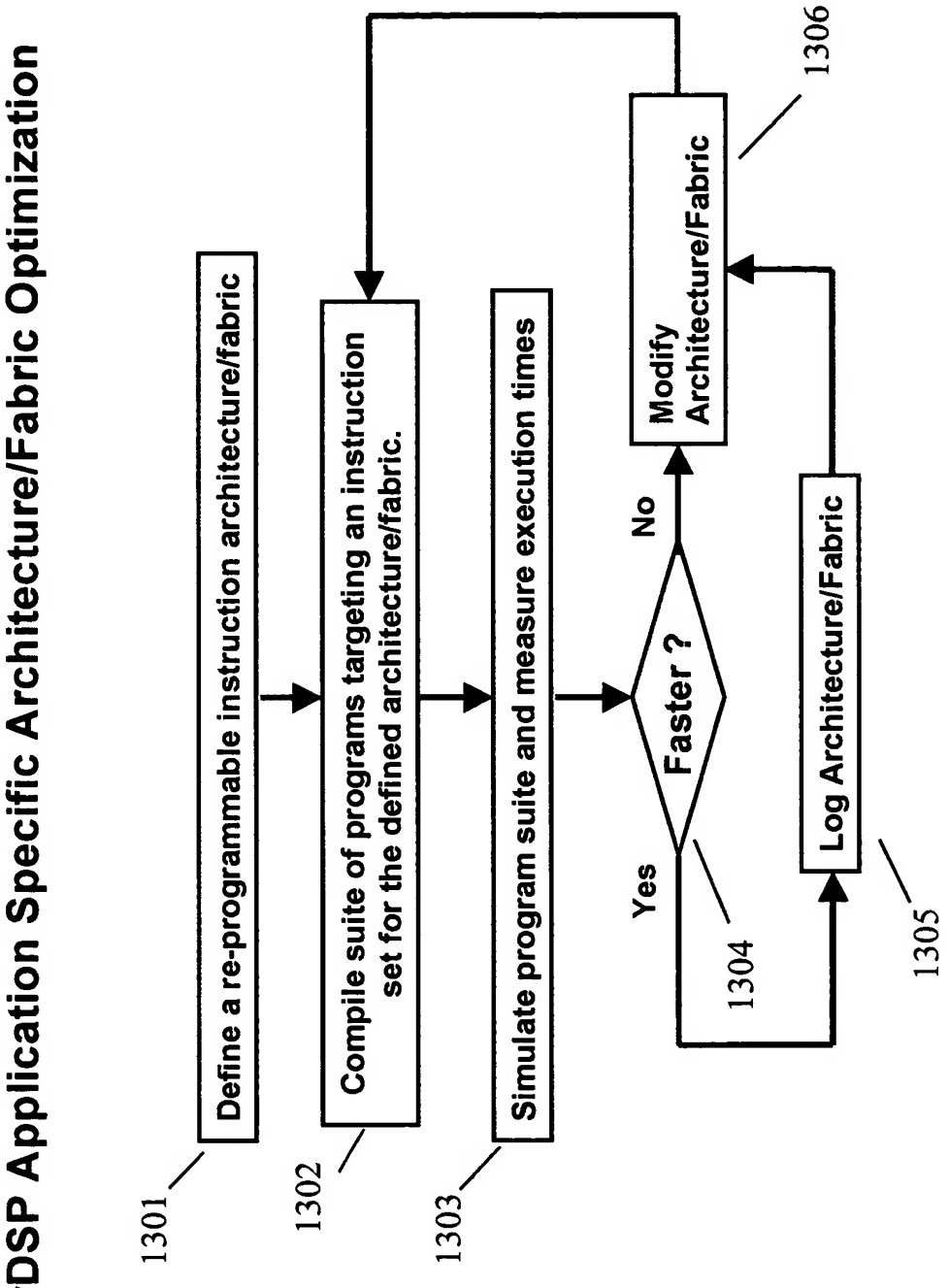
rDSP Application Specific Architecture/Fabric Optimization
Define a re-programmable instruction architecture/fabric
Compile suite of programs targeting an instruction set for the defined architecture/fabric.
Simulate program suite and measure execution times
Faster ?
Yes
No
Modify Architecture/Fabric
Log Architecture/Fabric
1301
1302
1303
1304
1305
1306

Figure 13

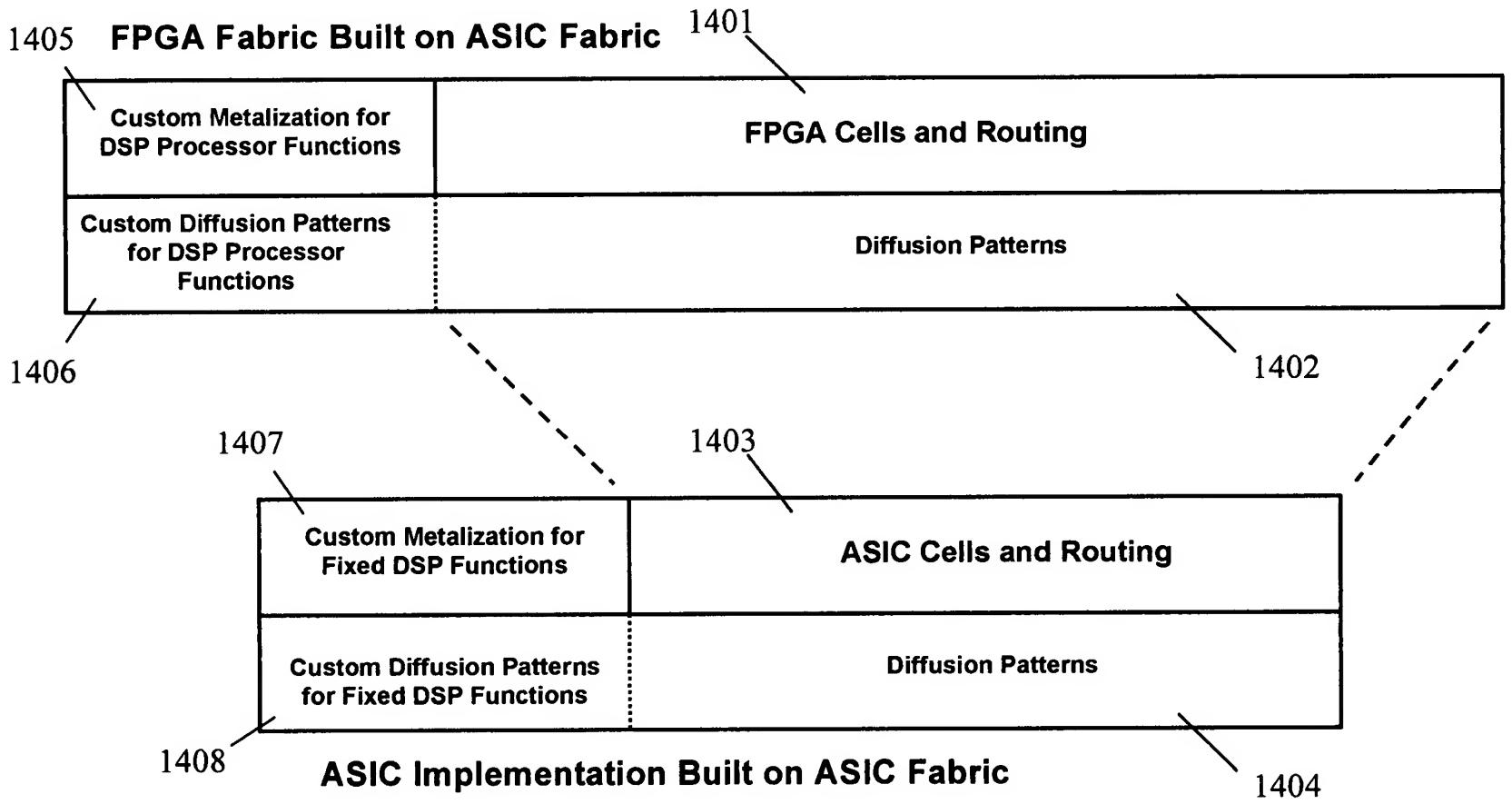

Figure 14

"Reprogrammable Instruction DSP"
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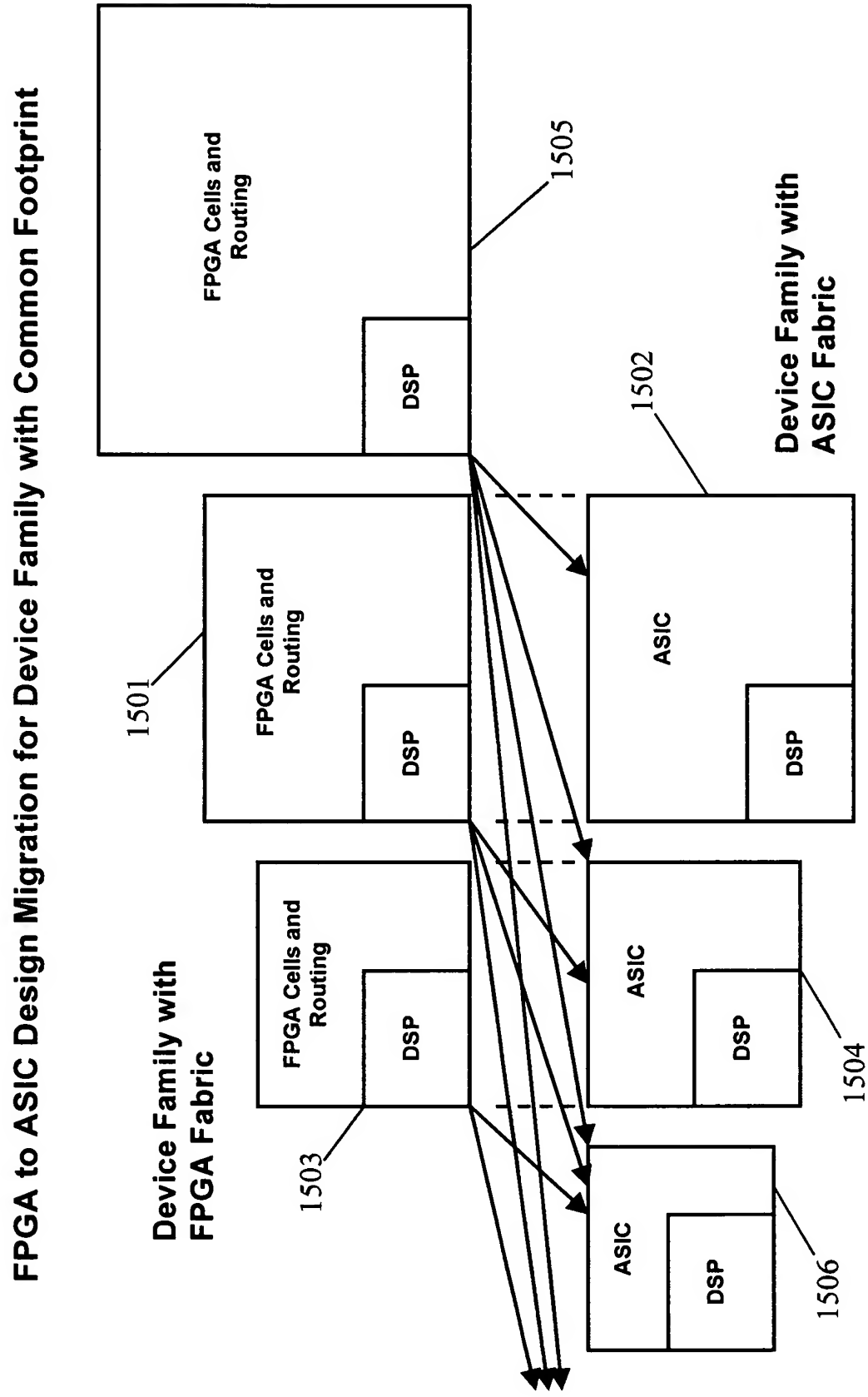
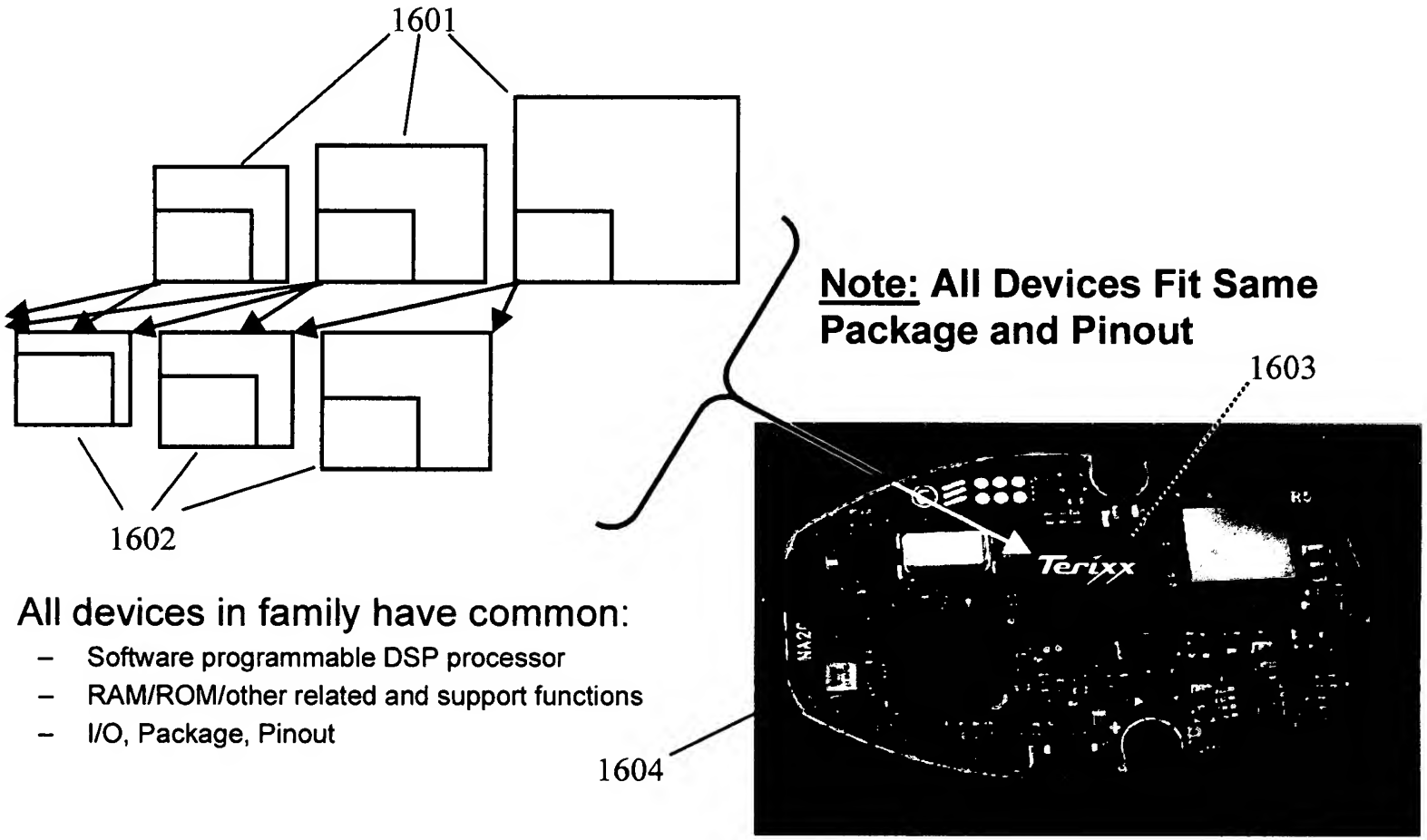

FPGA to ASIC Design Migration for Device Family with Common Footprint
Device Family with FPGA Fabric
Device Family with ASIC Fabric
FPGA Cells and Routing
DSP
ASIC
1501
1502
1503
1504
1505
1506

Figure 15

FPGA to ASIC Design Migration for Device Family with Common Footprint



- All devices in family have common:
  - Software programmable DSP processor
  - RAM/ROM/other related and support functions
  - I/O, Package, Pinout

Figure 16

"Reprogrammable Instruction DSP"
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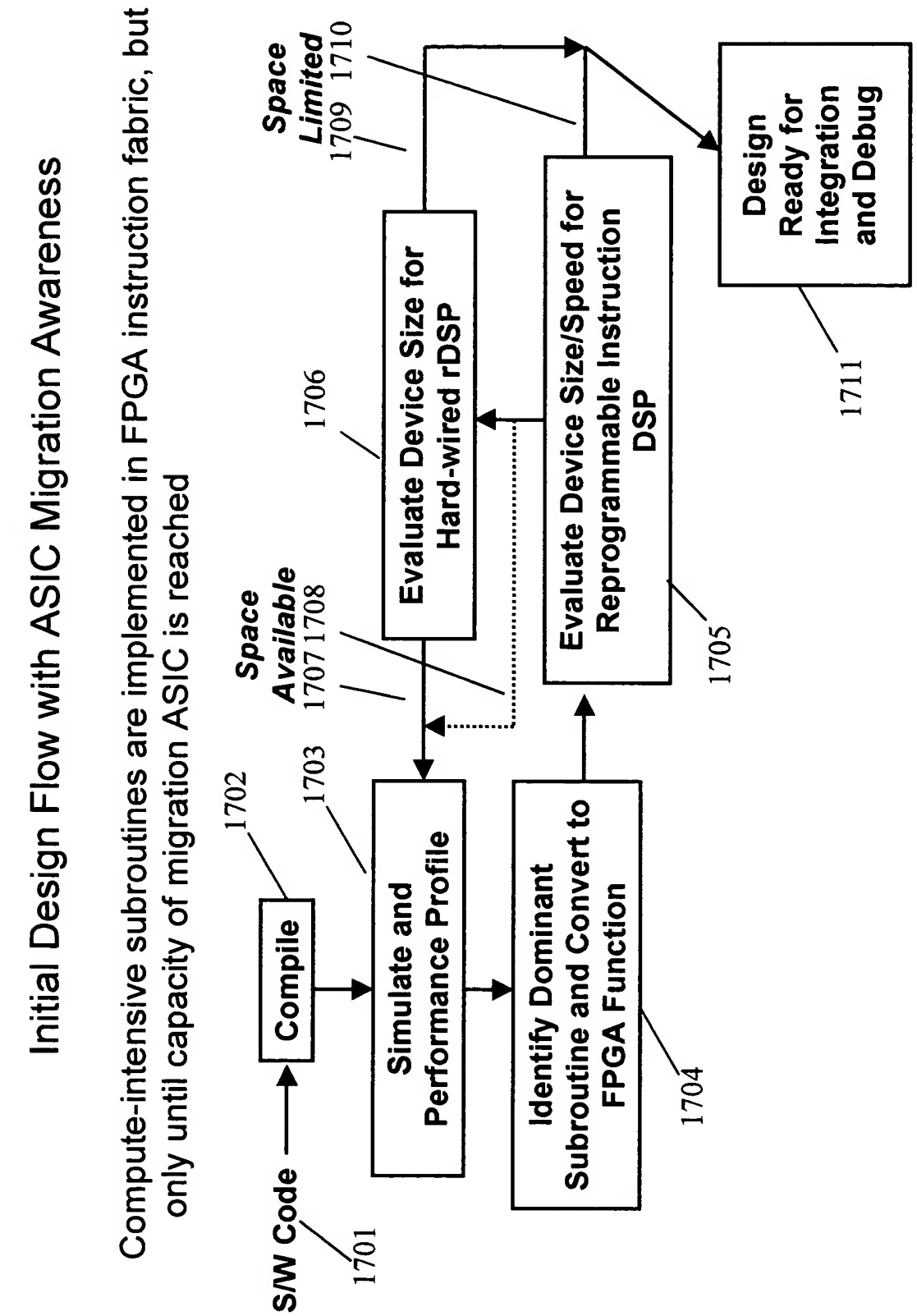
Initial Design Flow with ASIC Migration Awareness
Compute-intensive subroutines are implemented in FPGA instruction fabric, but only until capacity of migration ASIC is reached
S/W Code
1701
Compile
1702
Simulate and Performance Profile
1703
Space Available
1707 1708
Identify Dominant Subroutine and Convert to FPGA Function
1704
Evaluate Device Size for Hard-wired rDSP
1706
Space Limited
1709 1710
Evaluate Device Size/Speed for Reprogrammable Instruction DSP
1705
Design Ready for Integration and Debug
1711

Figure 17

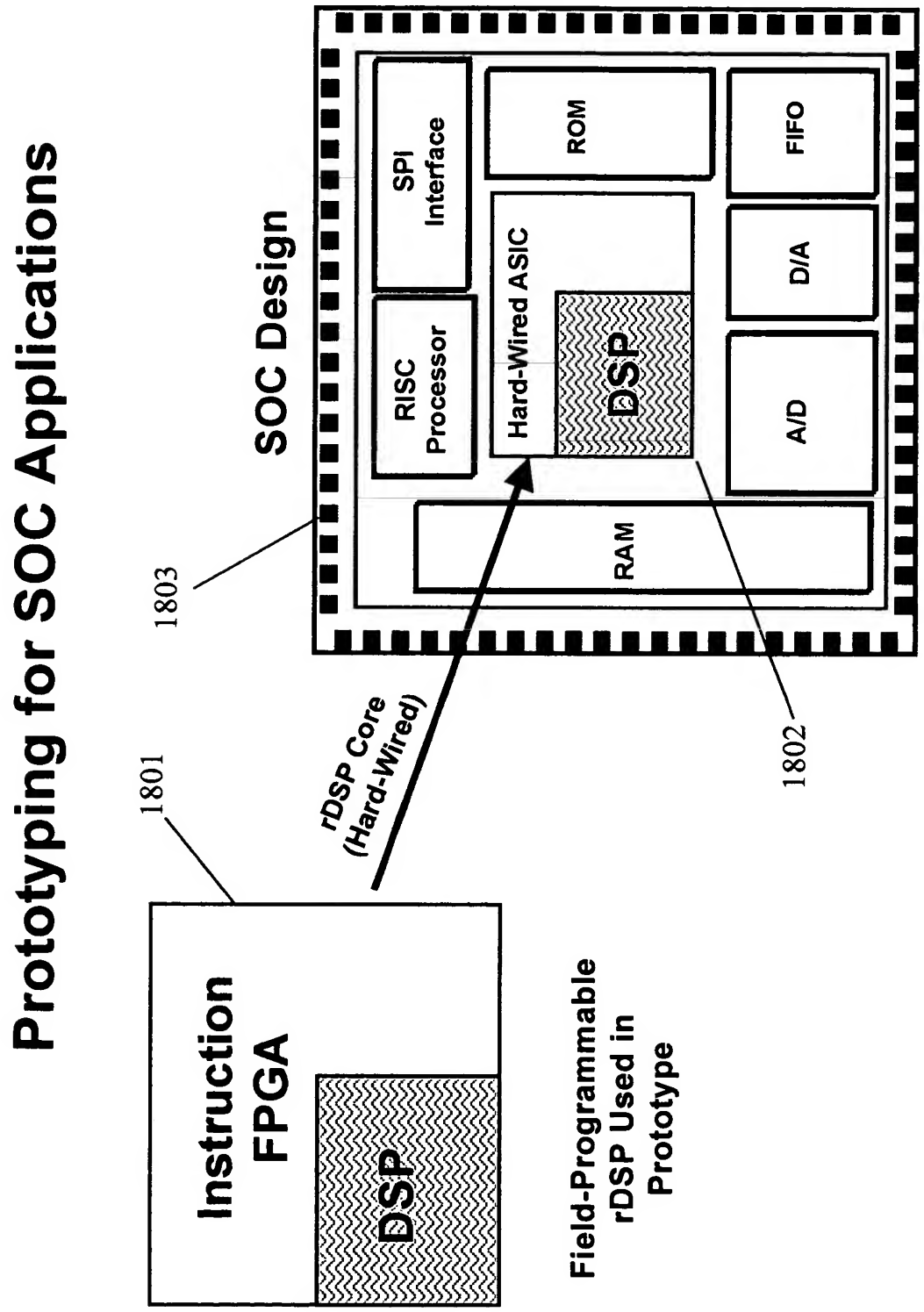
Prototyping for SOC Applications
SOC Design
1803
SPI Interface
ROM
FIFO
RISC Processor
Hard-Wired ASIC
DSP
D/A
A/D
RAM
1802
rDSP Core (Hard-Wired)
1801
Instruction FPGA
DSP
Field-Programmable rDSP Used in Prototype

Figure 18

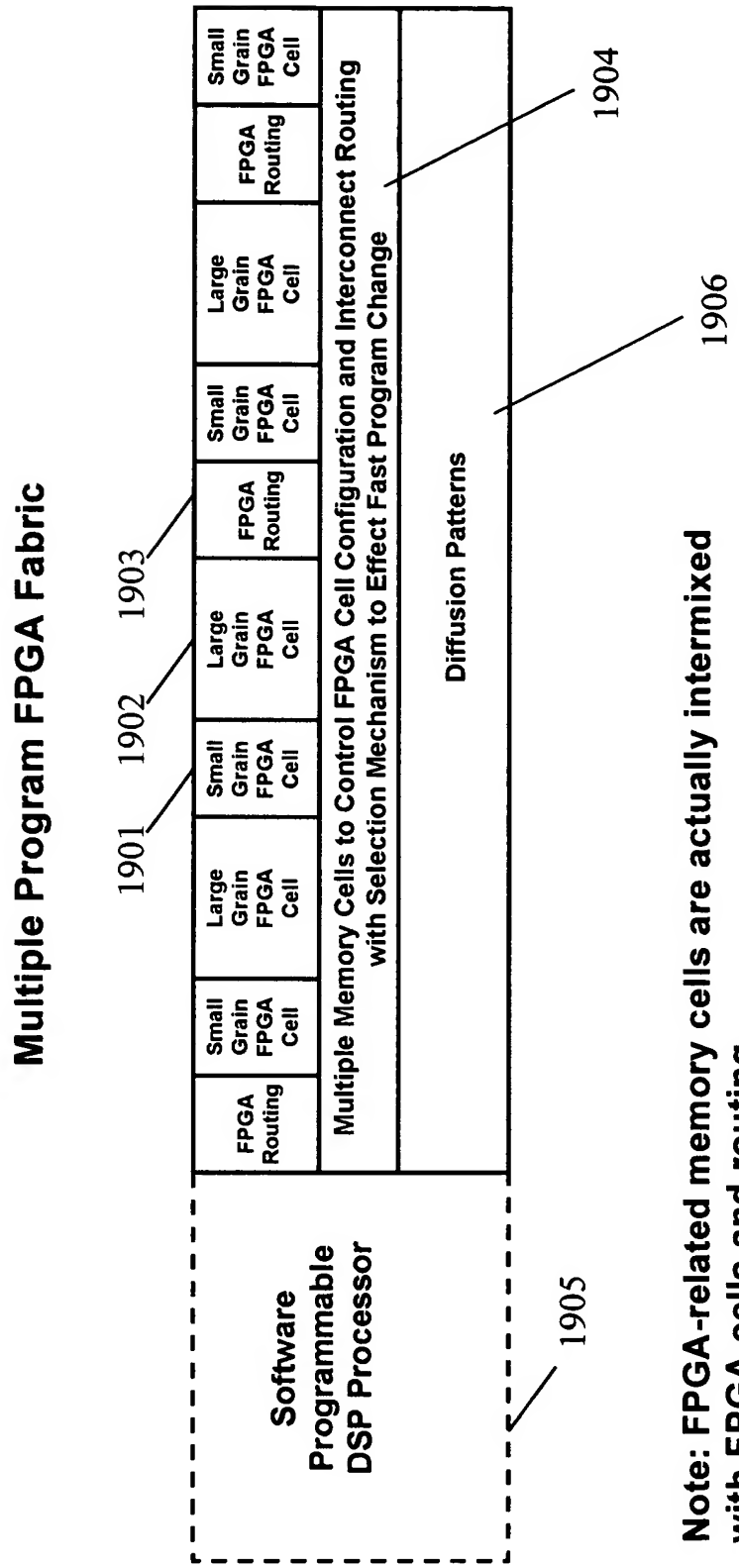
Multiple Program FPGA Fabric
Software Programmable DSP Processor
FPGA Routing
Small Grain FPGA Cell
Large Grain FPGA Cell
Small Grain FPGA Cell
Large Grain FPGA Cell
FPGA Routing
Small Grain FPGA Cell
Large Grain FPGA Cell
FPGA Routing
Small Grain FPGA Cell
Multiple Memory Cells to Control FPGA Cell Configuration and Interconnect Routing with Selection Mechanism to Effect Fast Program Change
Diffusion Patterns
1901
1902
1903
1904
1905
1906
Note: FPGA-related memory cells are actually intermixed with FPGA cells and routing.

Figure 19

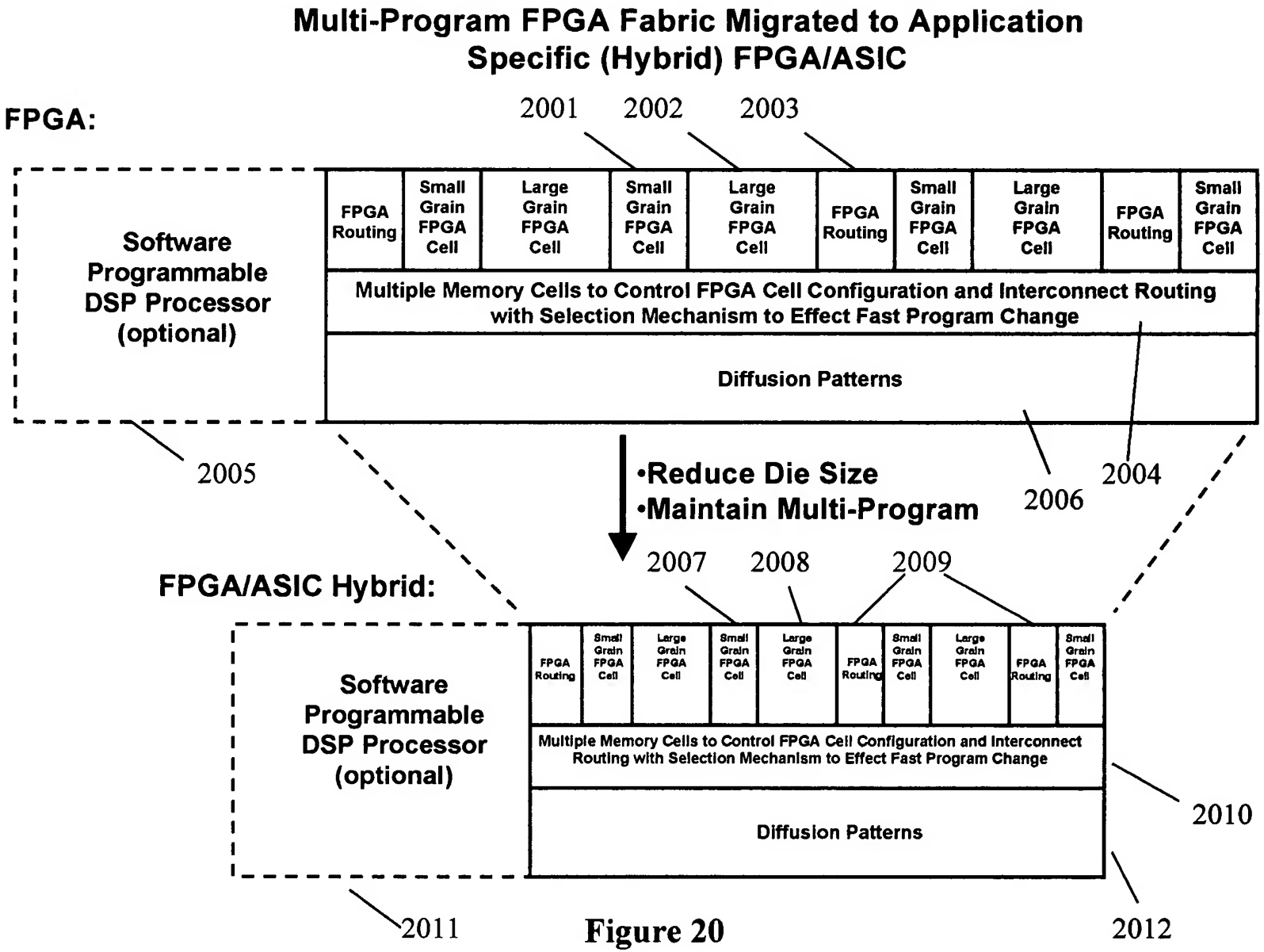

Figure 20

"Reprogrammabl Instruction DSP"
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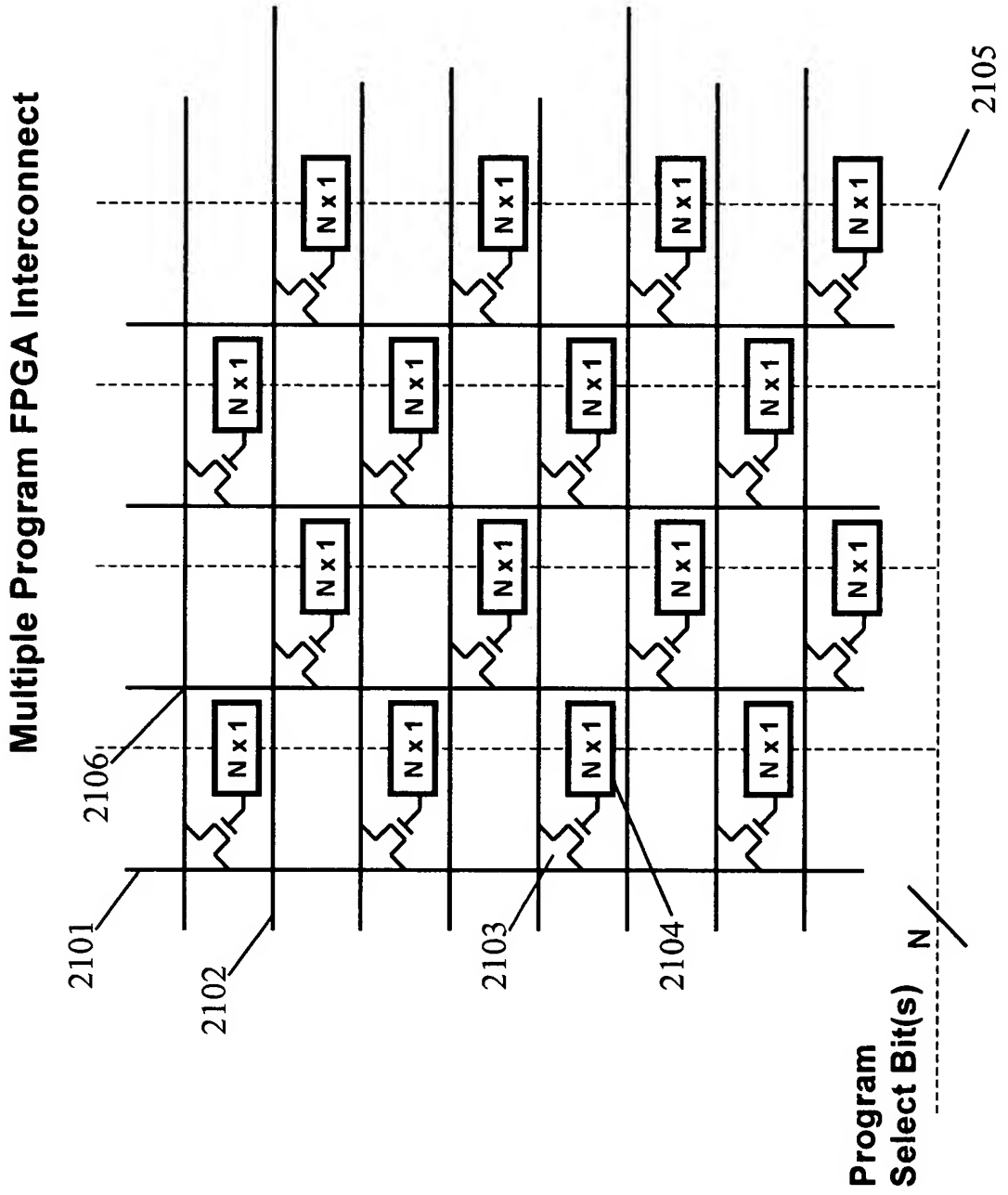

Multiple Program FPGA Interconnect
N x 1
2101
2102
2103
2104
2105
2106
Program
Select Bit(s)
N

Figure 21

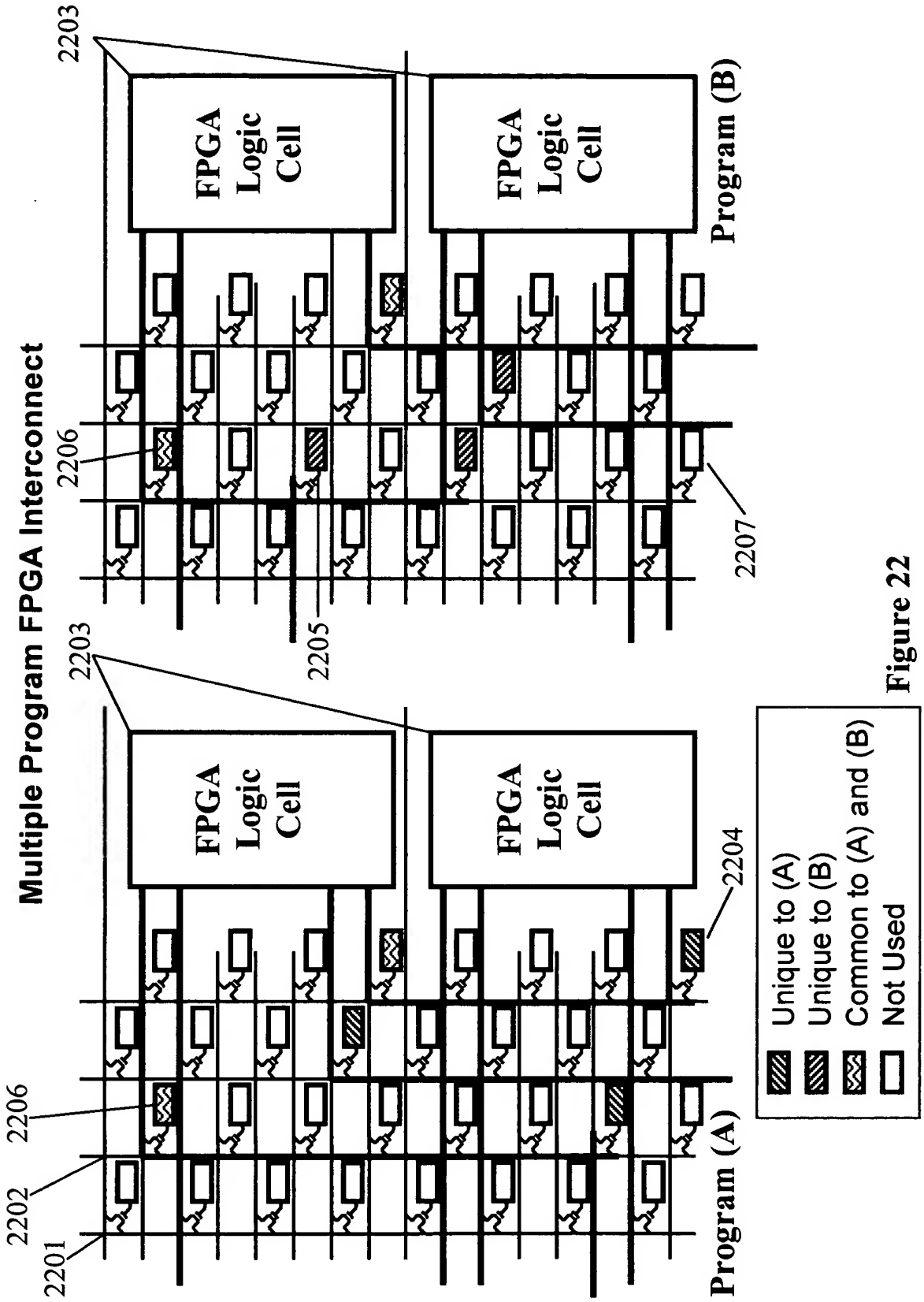
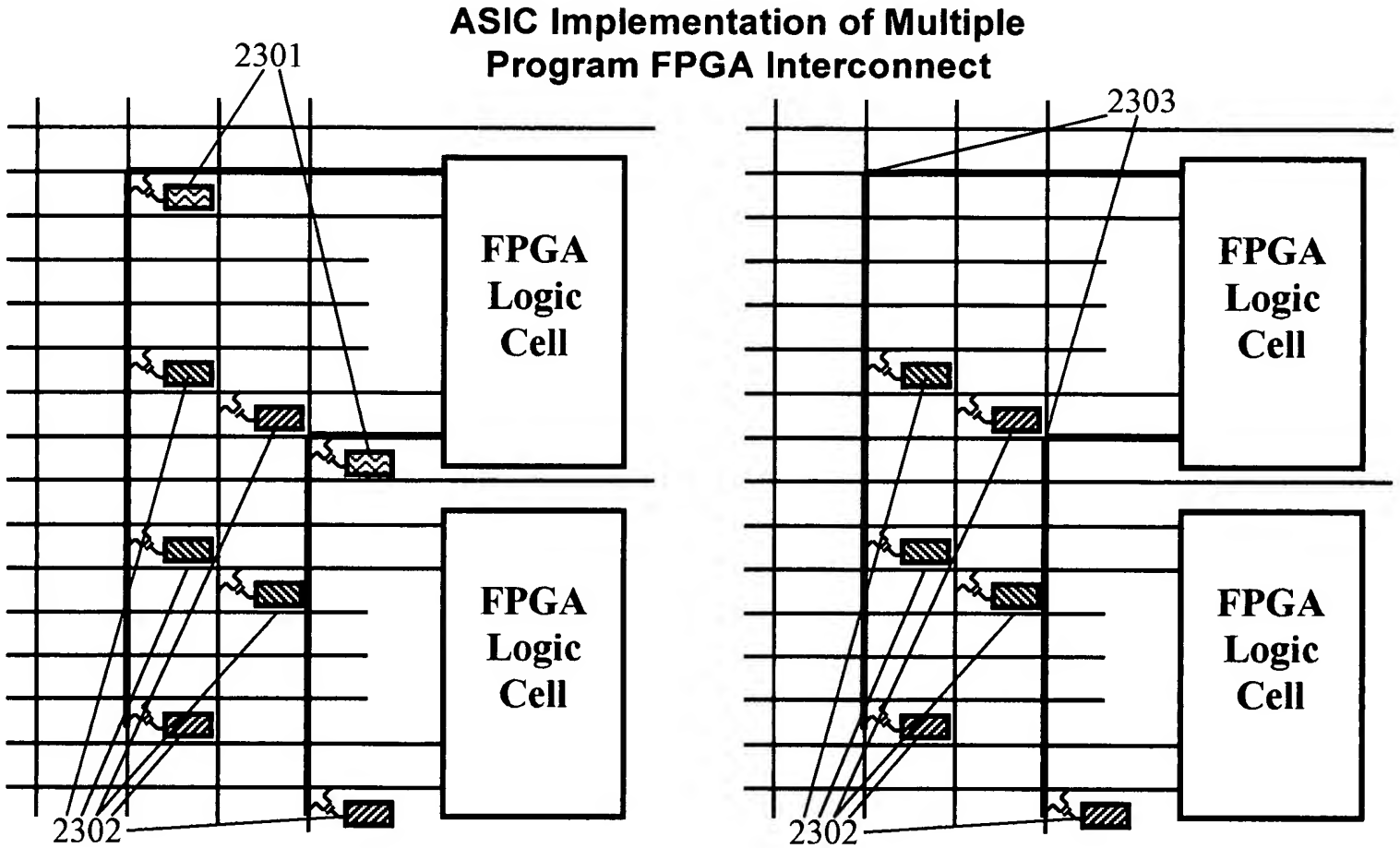

Multiple Program FPGA Interconnect
FPGA Logic Cell
FPGA Logic Cell
FPGA Logic Cell
FPGA Logic Cell
Program (A)
Program (B)
2201
2202
2203
2204
2205
2206
2207
Unique to (A)
Unique to (B)
Common to (A) and (B)
Not Used

Figure 22



(23-1) Utilized Connection Points

(23-2) Required Programmable Connection Points

Figure 23

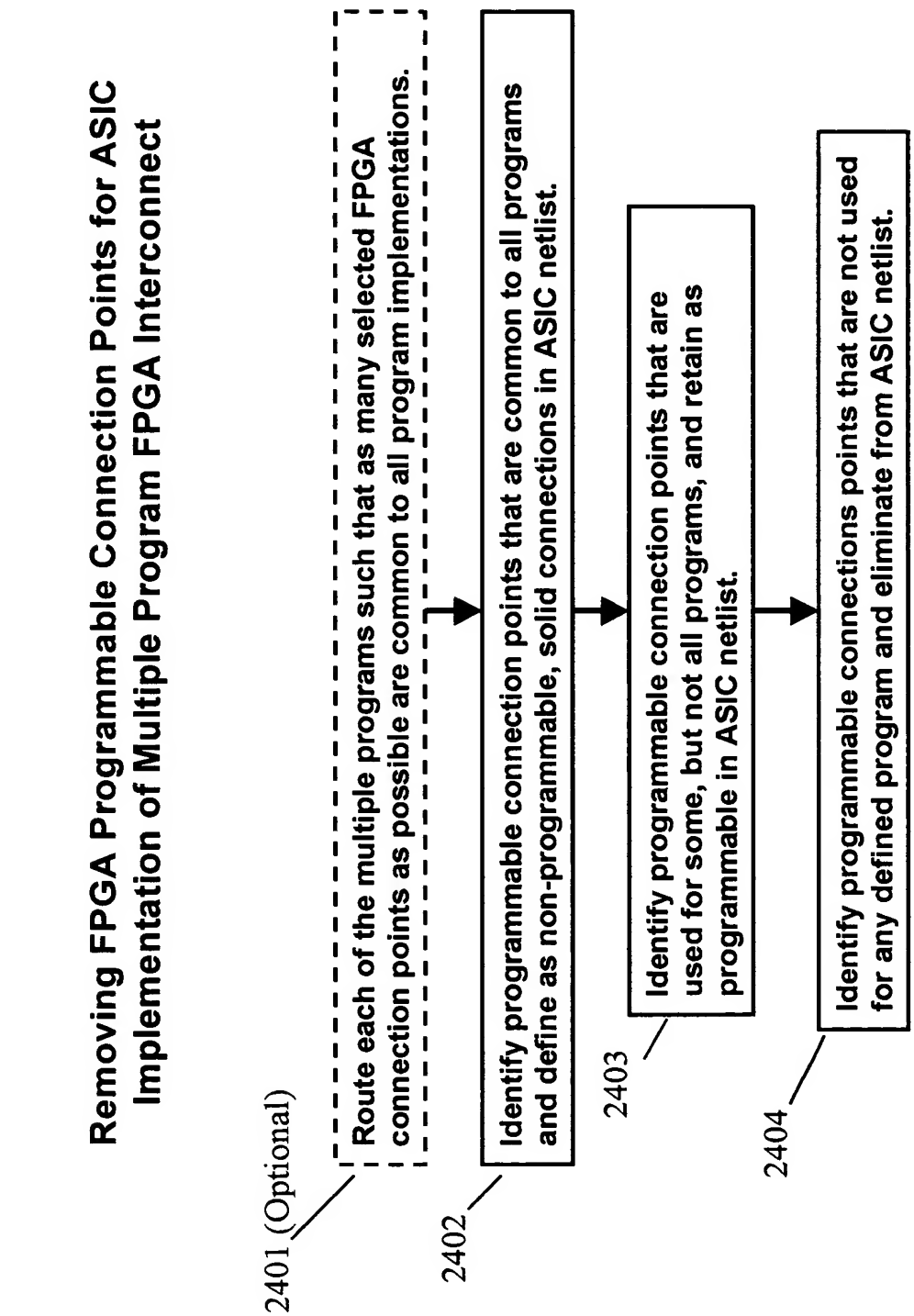

Removing FPGA Programmable Connection Points for ASIC Implementation of Multiple Program FPGA Interconnect
2401 (Optional)
Route each of the multiple programs such that as many selected FPGA connection points as possible are common to all program implementations.
2402
Identify programmable connection points that are common to all programs and define as non-programmable, solid connections in ASIC netlist.
2403
Identify programmable connection points that are used for some, but not all programs, and retain as programmable in ASIC netlist.
2404
Identify programmable connections points that are not used for any defined program and eliminate from ASIC netlist.

Figure 24